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ATTORNEY DOCKET NO. 10030540-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Robert S. Kolman

Serial No.: 10/686,332 **Examiner:** Bryan Bui

Filing Date: October 14, 2003 **Group Art Unit:** 2863

Title: DEVICE TESTING CONTROL

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on November 22, 2006 .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-1078** the sum of $500.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

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☒ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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☐ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

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Signature:

Respectfully submitted,

Robert S. Kolman

By

Gregory W. Osterloth
Attorney/Agent for Applicant(s)

Reg. No. 36,232

Date: January 23, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/686,332	Confirmation No. 7202
Appellants	:	Robert S. Kolman	
Filed	:	October 14, 2003	
TC/A.U.	:	2863	
Examiner	:	Bui, Bryan	
Docket No.	:	10030540-1	

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
PO Box 1450
Alexandria VA 22313-1450

APPEAL BRIEF

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Board of Patent Appeals and Interferences
United States Patent and Trademark Office
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Alexandria VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated August 22, 2005.

Appellants filed a Notice of Appeal on November 22, 2005.

Real Party in Interest

The real party in interest is Agilent Technologies, Inc., a Delaware corporation headquartered in Palo Alto, California.

Related Appeals and Interferences

There are no related appeals and/or interferences.

Status of Claims

Claims 1-19 remain pending. Of these, claims 1-4, 8, 9, 17 and 19 have been allowed. Claim 16 stands objected to as being dependent on a rejected base claim, but is otherwise allowable. Claims 10-15 and 18 stand rejected.

A copy of the claims is attached hereto in a Claims Appendix to this Appeal Brief.

Status of Amendments

All amendments have been entered.

Summary of Claimed Subject Matter

In a first embodiment (claim 10), a method implemented by a local controller (p. 5, par. [0012]-[0013]; 160, FIG. 2) of a test system comprises: 1) detecting (pp. 6-7, par. [0016]; 300, FIG. 3) a remote test instruction received (400, FIG. 4) from a remote controller (p. 6, par. [0015]; 200, FIG. 2); and 2) upon detecting the remote test instruction, switching (pp. 6-7, par. [0016]; p. 8, par. [0020]; 305, FIG. 3) from a control mode (pp. 5-6, par. [0014]; p. 9, par. [0025]), to control testing of a device (150, FIG. 2) and to initiate one or more test instructions to be applied to the device, to a slave mode (p. 8, par. [0021]; p. 9, par. [0024]) to pass through (405, FIG. 4) the remote test instruction to a tester (100, FIG. 2).

Grounds of Rejection to be Reviewed on Appeal

Whether claims 10-15 and 18 should be rejected under 35 USC 102(e) as being anticipated by Krech, Jr. et al (U.S. Pat. No. 6,779,140).

Argument

Claims 10-15 and 18 should not be rejected under 35 USC 102(e) as being anticipated by Krech, Jr. et al (U.S. Pat. No. 6,779,140; hereinafter "Krech")

Appellant's claim 10 recites:

> 10. A method, implemented by a local controller of a test system, comprising:
> detecting a remote test instruction received from a remote controller; and
> upon detecting the remote test instruction, switching from a control mode, to control testing of a device and to initiate one or more test instructions to be applied to the device, to a slave mode to pass through the remote test instruction to a tester.

In rejecting claim 10, the Examiner asserts:

> . . .Krech teach detecting a remote instruction received from a remote controller (figure 2, item 5 through bus controller 88, ring bus, microcontroller to detect remote instruction 22); upon detecting the remote test instruction, switching from a control mode (local control include control mode that executes test program to be applied to the device (figure 1, blocks 4a, 6a) to control testing of a device, to a slave mode (slave site controller in slave mode condition) to pass through the remote test instruction to a tester (title; figures 1, test system controller through system bus at blocks 2, 3 and 5a).
>
> 8/22/2005 Final Office Action, p. 2, sec. 4.

Appellant respectfully disagrees. To begin, Krech does not teach that any of the "ALU instructions 22" are remote test instructions received from a remote controller, as is recited in Appellant's claim 10. Rather, Krech teaches that:

> . . .The Ring Bus 85 is the mechanism by which the Test Site Controller communicates with the APG portion of the DUT tester 6. The Ring Bus 85 is coupled to a Micro-Controller Sequencer 19, which may be likened to a special purpose microprocessor. Using an address created by a Next Address Calculator 102, it fetches instructions from a program stored in a program memory, which may be either internal to the Micro-Controller Sequencer 19 (PGM SRAM 20) or external thereto (EXT. DRAM 21). Although these two memories appear to be addressed by what is essentially a logically common

address 63 that serves as a program counter (or, instruction fetch address), and either can be a source of programming to be executed, note that: (1) Only one of the memories performs instruction fetch memory cycles during any period of time; and (2) In fact they are addressed by electrically different signals. The SRAM is fast and allows genuine random access, but consumes valuable space within the Micro-Sequence Controller 19 (which is part of the large APG IC), so its size is limited. The external DRAM can be provided in adjustable amounts of considerable quantity, but is fast only when accessed in sequential chunks involving linear execution and no branching. Programming in the SRAM 20 is most often that which is intensely algorithmic, while the EXT. DRAM 21 is best suited for material not readily generated by algorithmic processes, such as initialization routines and random or irregular data.

Krech, col. 11, line 64 - col. 12, line 18.

The instruction word fetched and executed by the Micro-Controller Sequencer 19 is fairly wide: two hundred and eight bits. It consists of thirteen sixteen-bit fields. These fields often represent fetched instruction information for mechanisms that are outside the Micro-Controller Sequencer proper. Such fields are dedicated to their associated mechanisms. ***One set of ALU INSTRUCTIONS 22 are applied to a collection of eight sixteen-bit ALU's 24, while others are disbursed to various other mechanisms distributed throughout the DUT Tester.*** This latter situation is represented by the lines and legend "VARIOUS CONTROL VALUES & INSTRUCTIONS" 42.

Krech, col. 12, lines 27-38. Emphasis added.

The above-emphasized sentence is Krech's only discussion of the "ALU instructions 22"; and Appellant can find no mention that 1) any of the instructions 22 is a "remote test instruction received from a remote controller", or 2) any "remote test instruction received from a remote controller" is "passed through" the DUT tester 6. Rather, it appears that A) the instructions 22 are generated or fetched locally by the "micro-controller sequencer 19" of the "DUT tester 6", and B) none of the instructions that are written into the external DRAM 21 via the ring bus 85 are "detected" by the micro-controller sequencer 19, and are instead fetched in accord with a local program executed by the micro-controller sequencer 19.

Furthermore, Appellant cannot find any mention by Krech that, upon detecting a remote test instruction, a local controller of a test system switches from a "control

mode" to a "slave mode". Although Krech frequently discusses the operation of a test-site controller 6 in a "slave mode", Krech is talking about master-slave relationships between different *test-site controllers 6*, and these master-slave relationships do not appear to be for passing "remote test instructions" to a tester (i.e., in lieu of a local controller of a test system initiating one or more test instructions to be applied to a device). *See*, e.g., Krech, col. 10, lines 4-7.

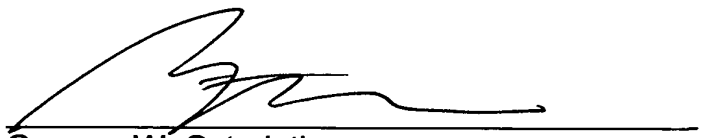
In light of the above arguments, Appellant believes the Examiner has failed to make a prima facie case for rejecting claim 10; and claim 10 should be allowed over Krech's teachings.

Appellant's claims 11-15 and 18 are believed to be allowable at least for the reason that they depend from appellant's claim 10.

2. Conclusion

In light of the above arguments, Appellant requests a reversal of the Examiner's rejections, and the allowance of his pending claims.

Respectfully submitted,
DAHL & OSTERLOTH, L.L.P.

By: 

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Claims Appendix

Claim 1: A system comprising:

a local controller having a slave mode and a control mode, when in the control mode, the local controller to control testing of a device and to initiate one or more test instructions to be applied to the device, and when in the slave mode, to pass through a remote test instruction received from a remote controller to a tester;

memory, communicatively coupled to the local controller, to receive the remote test instruction from the remote controller, the local controller obtaining the remote test instruction from the memory; and

the tester, communicatively coupled to the local controller, to apply one of the one or more test instructions and the remote test instruction to the device;

wherein the local controller polls the memory to detect the presence of the remote test instruction and switches from the control mode to the slave mode upon detecting the remote test instruction.

Claim 2: The system of claim 1, further comprising the remote controller, communicatively coupled to the local controller, to control testing of the plurality of devices when the local controller is in the slave mode.

Claim 3: The system of claim 1, wherein the local controller, when in the slave mode, is further to pass through a result of the remote test instruction to the remote controller.

Claim 4: A system comprising:

a local controller having,

a slave mode wherein the local controller i) controls testing of a device by initiating one or more test instructions to be applied to the device, and ii) manages at least one test result received from the tester as a result of applying the one or more test instructions; and

a slave mode wherein the local controller passes through a remote

test instruction received from a remote controller to a tester; and

the tester, communicatively coupled to the local controller, to apply one of the one or more test instructions and the remote test instruction to the device.

Claims 5-7 (canceled)

Claim 8: The system of claim 1, wherein the local controller is further to control testing of a second device and to initiate one or more test instructions for the second device when in the control mode and wherein the tester is further to apply the one or more test instructions for the second device to the second device.

Claim 9: The system of claim 1, wherein the tester comprises a system-on-a-chip (SOC) tester.

Claim 10: A method, implemented by a local controller of a test system, comprising:

detecting a remote test instruction received from a remote controller; and

upon detecting the remote test instruction, switching from a control mode, to control testing of a device and to initiate one or more test instructions to be applied to the device, to a slave mode to pass through the remote test instruction to a tester.

Claim 11: The method of claim 10, further comprising passing through the remote test instruction to the tester.

Claim 12: The method of claim 10, further comprising applying the remote test instruction to a device.

Claim 13: The method of claim 12, wherein applying the remote test instruction comprises applying the test instruction to a system-on-a-chip (SOC).

Claim 14: The method of claim 10, further comprising passing through a result of the remote test instruction to the remote controller.

Claim 15: The method of claim 14, further comprising locally compiling the result with a plurality of additional results passed through to the remote controller.

Claim 16: The method of claim 10, wherein detecting a remote test instruction comprises polling a memory shared with the remote controller.

Claim 17: A method, implemented by a local controller of a test system, comprising:

detecting a remote test instruction received from a remote controller by checking a semaphore; and

upon detecting the remote test instruction, switching from a control mode, to control testing of a device and to initiate one or more test instructions to be applied to the device, to a slave mode to pass through the remote test instruction to a tester.

Claim 18: The method of claim 10, wherein detecting a remote test instruction comprises detecting a test instruction to be applied to a system-on-a-chip (SOC).

Claim 19: A system, comprising:

a local controller having a slave mode and a control mode, when in the control mode, the local controller to control testing of a device and to initiate one or more test instructions to be applied to the device, and when in the slave mode, to pass through a remote test instruction received from a remote controller to a tester;

memory, communicatively coupled to the local controller, to receive the remote test instruction from the remote controller, the local controller obtaining the remote test instruction from the memory; and

the tester, communicatively coupled to the local controller, to apply one of the one or more test instructions and the remote test instruction to the device;

wherein the local controller detects the presence of the remote test instruction by checking a semaphore, and upon detecting the remote test instruction, switches from the control mode to the slave mode.

Evidence Appendix

None.

Related Proceedings Appendix

None.